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Title:

POWER SUPPLY APPARATUS VARING AN OUTPUT CONSTANT VOLTAGE IN RESPONSE TO A LOAD REQUIREMENT

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CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority under 35 USC §119 to Japanese patent application No. JPAP 2002-195406 filed July 4, 2002, and Japanese patent application No. JPAP 2002-249081, filed August 28, 2002, the entire contents of which are incorporated herein by reference.

FIELD OF THE INVENTION

[0002] The present invention relates to a power supply apparatus, and more particularly to a power supply apparatus capable of varying an output constant voltage in response to a control signal from a load circuit.

BACKGROUND OF THE INVENTION

[0003] Conventional power supply apparatus use a switching or series regulator on a power supply side for outputting a predetermined voltage required by a load side. As shown in FIG. 1, a background power supply apparatus 100 has a feedback configuration to return an output voltage Vo of a DC-to-DC converter, to divide the output voltage Vo with a voltage divider 101 into a divided voltage Vd, and to compare the divided voltage Vd with a predetermined reference voltage Vr.

[0004] Due to a recent trend, however, the voltage required by the load side has been reduced, and the power supply apparatus is consequently required to change the output voltage of the switching or series regulator. Also, the power supply apparatus itself needs to be changed when a required power supply voltage value is changed by, for example, the replacement of a component used in the load side of a system after the power supply apparatus is installed into the system.

[0005] In view of the foregoing, it is desirable to change a level of an output constant voltage in response to a control signal sent from a load side.

SUMMARY OF THE INVENTION

[0006] In one example, a novel power supply apparatus includes an input terminal, an output voltage generator, an output terminal, a reference voltage generator, a voltage divider, and a voltage control circuit. The input terminal is supplied with an input voltage from a direct current power source. The output voltage generator is configured to generate a constant output voltage based on the input voltage. The output terminal outputs the constant output voltage. The reference voltage generator is configured to generate a reference voltage. The voltage divider has an output and is configured to divide the constant output voltage into a divided voltage output from the output in accordance with a voltage dividing ratio variable in response to an externally-input control signal. The voltage control circuit is configured to control the output voltage generator to regulate the constant output voltage such that the divided voltage from the voltage divider is equalized to the reference voltage.

[0007] The voltage divider may include a first resistor circuit, a first switch circuit, a second resistor circuit, a second switch circuit, and a switch control circuit. The first resistor circuit includes a plurality of resistors connected in series between the output terminal and the output point of the voltage divider. The first switch circuit is configured to make a short circuit in at least one of the plurality of resistors included in the first resistor circuit in response to an input control signal. The second resistor circuit includes a plurality of resistors. The second switch circuit is configured to connect in parallel at least one of the plurality of resistors included in the second resistor circuit between the output point of the voltage divider and a common ground of the direct current power source in response to the input control signal. The switch control circuit is configured to generate the input control signal in response to the externally-input control signal and to control the first and second switch circuits with the input control signal to change the voltage dividing ratio.

[0008] The voltage divider may include a first resistor circuit, a first switch circuit, a second resistor circuit, a second switch circuit, and a switch control circuit. The first resistor circuit includes a plurality of resistors. The first switch circuit is configured to connect in parallel at least one of the plurality of resistors included in the first resistor circuit between the output terminal and the output point of the voltage divider in response to an input control signal. The second resistor circuit includes a plurality of resistors connected in series between the output point of the voltage divider and a common ground of the direct current power source. The second switch circuit is configured to make a short circuit in at least one of the plurality of resistors included in the second resistor circuit in response to the input control signal. The switch control circuit is configured to generate the input control signal in response to the externally-input control signal and to control the first and second switch circuits with the input control signal to change the voltage dividing ratio.

[0009] The output voltage generator may include a switching transistor performing a switching operation for outputting the input voltage applied by the direct current power source in accordance with a control signal from the voltage control circuit, and the voltage control circuit may include an error amplifier, a control circuit, and a smoothing circuit. The error amplifier amplifies an error of the divided voltage output from the output point of the voltage divider relative to the reference voltage. The control circuit is configured to generate the control signal in accordance with an output signal from the error amplifier to control the switching operation of the switching transistor. The smoothing circuit is configured to smooth an output signal from the switching transistor and to output to the output terminal.

[0010] The reference voltage generator, the voltage divider, the error amplifier, and the control circuit may be integrated into a single integrated circuit.

[0011] The reference voltage generator, the switching transistor, the voltage divider, the error amplifier, and the control circuit may be integrated into a single integrated circuit.

[0012] The smoothing circuit may include a transistor which is operated and controlled by the control circuit to function as a flywheel diode, and the transistor, the switching transistor, the voltage divider, the error amplifier, the smoothing transistor and the control circuit may be integrated into a single integrated circuit.

[0013] The output voltage generator may include an output control transistor controlling an output of a current applied by the direct current power source in accordance with a control signal from the voltage control circuit, and the voltage control circuit may include an error amplifier controlling an operation of the output control transistor such that the divided voltage of the voltage divider is equalized to the reference voltage.

[0014] The reference voltage generator, the voltage divider, and the error amplifier may be integrated into a single integrated circuit.

[0015] The reference voltage generator, the voltage divider, the error amplifier, and the output control transistor may be integrated into a single integrated circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] A more complete appreciation of the disclosure and many of the attendant advantages thereof will be readily obtained as the same becomes better understood by reference to the following detailed description when considered in connection with the accompanying drawings, wherein:

[0017] FIG. 1 is a circuit diagram of a conventional power supply apparatus;

[0018] FIG. 2 is an exemplary circuit diagram of a power supply apparatus according to a preferred embodiment of the present invention;

[0019] FIG. 3 is an exemplary circuit diagram of a voltage dividing circuit included in the power supply apparatus of FIG. 2;

[0020] FIG. 4 is an exemplary circuit diagram of the voltage dividing circuit when in FIG. 3 is two;

[0021] FIG. 5 is an exemplary circuit diagram of a power supply apparatus according to another preferred embodiment of the present invention;

[0022] FIG. 6 is an exemplary circuit diagram of a power supply apparatus according to another preferred embodiment of the present invention;

[0023] FIG. 7 is an exemplary circuit diagram of a power supply apparatus according to another preferred embodiment of the present invention;

[0024] FIG. 8 is an exemplary circuit diagram of a power supply apparatus according to another preferred embodiment of the present invention;

[0025] FIG. 9 is an exemplary circuit diagram of a voltage dividing circuit included in the power supply apparatus of FIG. 7; and

[0026] FIG. 10 is an exemplary circuit diagram of the voltage dividing circuit when in FIG. 9 is two.

DETAILED DESCRIPTION OF THE INVENTION

[0027] In describing preferred embodiments illustrated in the drawings, specific terminology is employed for the sake of clarity. However, the disclosure of this patent specification is not intended to be limited to the specific terminology so selected and it is to be understood that each specific element includes all technical equivalents that operate in a similar manner. Referring now to the drawings, wherein like reference numerals designate identical or corresponding parts throughout the several views, particularly to FIG. 2, a power supply apparatus 1 according to a preferred embodiment of the present invention is explained. The power supply apparatus 1 of FIG. 2 is an exemplary power supply apparatus provided with a DC-to-DC (direct current to direct current) converter including a voltage-step-down-type switching regulator.

[0028] As shown in FIG. 2, the power supply apparatus 1 is connected to a direct current power source 10, and includes a switching transistor 2, a smoothing circuit 3, a reference voltage generator 4, a voltage dividing circuit 5, an error amplifier 6, and a control circuit 7. The current power source 10 includes a battery and the like and applies a voltage Vbat to the switching transistor 2 through an input terminal IN of the power supply apparatus 1. The switching transistor 2 includes a P-channel MOS (metal oxide semiconductor) transistor (hereinafter referred to as a PMOS transistor) which outputs the voltage Vbat applied thereto by the direct current power source 10. The smoothing circuit 3 smoothes the signal output from the switching transistor 2 and outputs the signal having a voltage Vo to an output terminal OUT. The reference voltage generator 4 generates a reference voltage Vr having a predetermined voltage value. The voltage dividing circuit 5 divides the voltage Vo and outputs a divided voltage Vd. The error amplifier 6 amplifies an error of the divided voltage Vd relative to the reference voltage Vr. The control circuit 7 controls the switching of the switching transistor 2 in accordance with the signal output from the error amplifier 6.

[0029] The output voltage Vo is divided by the voltage dividing circuit 5, and the difference between the resultant divided voltage Vd, which is regarded as an error, is amplified by the error amplifier 6. The control circuit 7 includes an oscillator for generating, for example, a pulse signal having a triangular waveform and a comparator. In the control circuit 7, the comparator compares the voltage of the signal output from the oscillator with the voltage of the signal output from the error amplifier 6. In accordance with a result of the comparison, the comparator controls a time that the switching transistor 2 is being turned on. The signal output from the switching transistor 2 is smoothed and output as the voltage Vo, by the smoothing circuit 3 which includes a flywheel diode D1, an electric coil L1, and a capacitor C1.

[0030] The voltage dividing circuit 5 includes a voltage divider 11 and a switching controller 12. The voltage divider 11 switches a dividing ratio in accordance with an input control signal, and accordingly generates and outputs the divided voltage Vd. The switching controller 12 controls the switching of the dividing ratio of the voltage

divider 11 in accordance with a voltage switching signal Sc which is externally input thereto.

[0031] FIG. 3 breaks down the voltage divider 11 of the voltage dividing circuit 5, and an exemplary operation of the voltage dividing circuit 5 is explained with reference to FIG. 3. The voltage divider 11 includes n resistors in series referred to as resistors RA1 – RAn, n resistors referred to as resistors RB1 – RBn, (n-1) PMOS transistors referred to as PMOS transistors QP1 – QPn-1, n N-channel MOS transistors referred to as NMOS transistors QN1 – QNn, and a capacitor 16. The resistors RA1 – RAn are configured as a first resistor circuit, the resistors RB1 – RBn are configured as a second resistor circuit, the PMOS transistors QP1 – QPn-1 are configured as a first switching circuit, and the NMOS transistors QN1 – QNn are configured as a second switching circuit.

[0032] The resistors RA1 – RAn are connected in series between the terminal OUT of the power supply apparatus 1 and the output terminal 15. The PMOS transistors QP1 – QPn are coupled to the resistors RA1 – RAn, respectively, to form n sets of transistor-resistor parallel circuits, which are connected in series between the output terminal 15 and a ground. The switching controller 12 generates control signals SP1 – SPn based on the voltage switching signal Sc, and applies the control signals SP1 – SPn-1 to gates of the PMOS transistors QP1 – QPn-1, respectively.

[0033] A capacitor 16 is also connected between the terminal OUT of the power supply apparatus 1 and the output terminal 15. The NMOS transistors QN1 – QNn are coupled to the resistors RB1 – RBn, respectively, to form n sets of transistor-resistor series circuits, which are connected in parallel between the output terminal 15 and a ground. The control signals SP1 – SPn of the switching controller 12 are also applied to gates of the PMOS transistors QN1 – QNn, respectively.

[0034] The switching controller 12 raises one of the control signals SP1 – SPn to a predetermined high level (hereinafter referred to as a level H) and drops the rest down to a predetermined low level (hereinafter referred to as a level L) in accordance with

the externally supplied input voltage switching signal Sc. For example, when the control signal SPm is raised to the level H and the rest of the control signals are lowered to the level L, the PMOS transistor QPm is selected among the PMOS transistors QP1 – QPn-1 to be turned off to become non-conductive and the rest of the PMOS transistors are turned on to be conductive, where m is an integer between 1 and n-1. At the same time, the NMOS transistor QNm is selected among the NMOS transistors QN1 – QNn to be turned on to be conductive and the rest of the NMOS transistors are turned off to become non-conductive. Thereby, the resistors RAm and RAn are connected in series between the output terminal OUT and the output terminal 15, and the resistor RBm is connected between the output terminal 15 and the ground.

[0035] When the above-described conditions are established, the divided voltage Vd is expressed by a first equation; Vd=(Vo x RBm)/(RAm+RAn+RBm), where RAm, RBm, and RAn represent values of the resistors RAm, RBm, and RAn, respectively.

[0036] The input voltages to the inverse and non-inverse input terminals of the error amplifier 6, which are Vd and Vr, respectively, are equalized due to a phenomenon called an imaginary short occurring therebetween. That is, in this case, a relationship between Vd and Vr is expressed as Vd=Vr. Therefore, the above first equation can be modified as; Vo=Vr x (RAm+RAn+RBm)/RBm.

[0037] For another example, when the control signal SPn is raised to the level H and the control signals SP1 – SPn-1 are lowered to the level L, the PMOS transistors QP1 – QPn-1 are turned on to be conductive. At the same time, the NMOS transistor QNn is turned on to be conductive and the rest of the NMOS transistors QN1 – QNn-1 are turned off to be non-conductive. Thereby, the resistor RAn is connected between the output terminal OUT and the output terminal 15, and the resistor RBn is connected between the output terminal 15 and the ground.

[0038] Under the above-mentioned conditions, the divided voltage Vd is expressed by a second equation; Vd=(Vo x RBn)/(RAn+RBn), where RBn represents a value of the resistor RBn.

[0039] The input voltages to the inverse and non-inverse input terminals of the error amplifier 6, which are Vd and Vr, respectively, are equalized due to the imaginary short phenomenon occurring therebetween. That is, in this case, a relationship between Vd and Vr is expressed as Vd=Vr. Therefore, the above second equation can be modified as; Vo=Vr x (RAn+RBn)/RBn.

[0040] In this way, the voltage divider 11 can vary the value of the output voltage Vo in accordance with the voltage switching signal Sc. In other words, a desirable value of the output voltage Vo can be obtained from the voltage divider 11 by suitably selecting the voltage switching signal Sc.

[0041] FIG. 4 shows an exemplary circuit of the voltage dividing circuit 5 when n is two. In the voltage dividing circuit 5 of FIG. 4, the resistors RA1 and RA2 are connected in series between the output terminal OUT and the output terminal 15. The PMOS transistor QP1 is connected parallel to the resistor RA1 and the capacitor 16 is connected between the output terminal OUT and the output terminal 15.

[0042] Further, in the voltage dividing circuit 5 of FIG. 4, the NMOS transistors QN1 and QN2 are coupled to the resistors RB1 and RB2, respectively, to form two sets of transistor-resistor series circuits, which are connected in parallel between the output terminal 15 and the ground. The switching controller 12 includes an inverter 17, and generates the control signals SP1 and SP2 based on the voltage switching signal Sc. The control signal SP1 is a straight signal of the voltage switching signal Sc and the control signal SP2 is an inverted signal of the voltage switching signal Sc. The control signal SP1 is applied to the gates of the PMOS transistor QP1 and the NMOS transistor QN1, and the control signal SP2 is applied to the gate of the NMOS transistor QN2.

[0043] In the voltage dividing circuit 5 of FIG. 4, the output voltage Vo based on the above modified first equation can be expressed as;
Vo=Vr x (RA1+RA2+RB1)/RB1.

[0044] Also, in the voltage dividing circuit 5 of FIG. 4, the output voltage Vo based on the above modified second equation can be expressed as;

$Vo=Vr \times (RA2+RB2)/RB2$.

[0045] In the power supply apparatus 1 of FIG. 2, the reference voltage generator 4, the voltage dividing circuit 5, the error amplifier 6, and the control circuit 7 are integrated into one IC (integrated circuit) chip. It is possible to further integrate the switching transistor 2 into that IC chip.

[0046] It is also possible to substitute an NMOS transistor for the flywheel diode D1. FIG. 5 shows a power supply apparatus 1a, which is a first exemplary alternative embodiment based on the power supply apparatus 1 of FIG. 2, in which the flywheel diode D1 is substituted by an NMOS transistor 21. In this case, it becomes possible to integrate the switching transistor 2, the reference voltage generator 4, the voltage dividing circuit 5, the error amplifier 6, the control circuit 7, and the NMOS transistor 21 into one IC (integrated circuit) chip.

[0047] FIG. 6 shows a power supply apparatus 1b, which is a second exemplary alternative embodiment based on the power supply apparatus 1 of FIG. 2. The power supply apparatus 1b of FIG. 6 is an exemplary power supply apparatus provided with a DC-to-DC (direct current to direct current) converter including a voltage-step-up-type switching regulator.

[0048] The power supply apparatus 1b of FIG. 6 is similar to the power supply apparatus 1 of FIG. 2, except for a switching regulator 31, a smoothing circuit 32, and a control circuit 33. The switching regulator 31 includes an NMOS transistor and performs a switching operation in accordance with a control signal input to a gate thereof. The smoothing circuit 32 smoothes the signal output from the switching transistor 31 and outputs a resultant signal having an output voltage Vo to the output terminal OUT. The control circuit 33 controls the switching operation of the switching transistor 31 in accordance with the signal output from the error amplifier 6.

[0049] The output voltage Vo output to the output terminal OUT is divided by the voltage dividing circuit 5, and the difference between the resultant divided voltage Vd, which is regarded as an error, is amplified by the error amplifier 6. The control circuit 33 includes an oscillator for generating, for example, a pulse signal having a triangular waveform and a comparator. In the control circuit 33, the comparator compares the voltage of the signal output from the oscillator with the voltage of the signal output from the error amplifier 6. In accordance with a result of the comparison, the comparator controls a time that the switching transistor 31 is being turned on. The signal output from the switching transistor 31 is smoothed and output as the voltage Vo, by the smoothing circuit 32, which includes a rectifying diode D2, an electric coil L2, and a capacitor C2.

[0050] In the power supply apparatus 1b of FIG. 6, the reference voltage generator 4, the voltage dividing circuit 5, the error amplifier 6, and the control circuit 33 are integrated into one IC (integrated circuit) chip. It is possible to further integrate the switching transistor 31 into that IC chip.

[0051] FIG. 7 shows a power supply apparatus 1c, which is a third exemplary alternative embodiment based on the power supply apparatus 1 of FIG. 2. The power supply apparatus 1c of FIG. 7 is an exemplary power supply apparatus provided with a DC-to-DC (direct current to direct current) converter including a series regulator instead of a switching regulator.

[0052] The power supply apparatus 1c of FIG. 7 is similar to the power supply apparatus 1 of FIG. 2, except for an output control transistor 41 and a capacitor 42. The output control transistor 41 includes a PMOS transistor and outputs to the output terminal OUT a current in accordance with a voltage input to a gate thereof from the error amplifier 6. The capacitor 42 stabilizes an output voltage Vo output through the output terminal OUT.

[0053] The output voltage Vo output to the output terminal OUT is divided by the voltage dividing circuit 5, and the difference between the resultant divided voltage Vd, which is regarded as an error, is amplified by the error amplifier 6. The error amplifier

6 outputs a resultant voltage to a gate of the output control transistor 41. The error amplifier 6 thus controls the operation of the output control transistor 41 so as to regulate the output voltage Vo to a predetermined preferable voltage.

[0054] In the power supply apparatus 1c of FIG. 7, the reference voltage generator 4, the voltage dividing circuit 5, and the error amplifier 6 are integrated into one IC (integrated circuit) chip. It is possible to further integrate the output control transistor 41 into that IC chip.

[0055] In the case of the power supply apparatus 1 of FIG. 1, the switching controller 12 of the voltage dividing circuit 5 is configured to cause one of the PMOS transistors QP1 – QPn-1 to turn exclusively off or every one of the PMOS transistors QP1 – QPn-1 to turn on and one of the NMOS transistors QN1 – QNn to turn exclusively on, in accordance with the externally input voltage switching signal Sc, as one example. This setting of the switching controller 12 in the power supply apparatus 1 can also be applied to the switching controller 12 of the power supply apparatus 1c, as one example.

[0056] As one exemplary alternative, in the power supply apparatus 1c, the switching controller 12 of the voltage dividing circuit 5 may cause more than one of the PMOS transistors QP1 – QPn-1 to turn off simultaneously and more than one of the NMOS transistors QN1 – QNn to turn on simultaneously, in accordance with the externally input voltage switching signal Sc.

[0057] As another exemplary alternative, in the power supply apparatus 1c, the switching controller 12 of the voltage dividing circuit 5 may cause one of the PMOS transistors QP1 – QPn-1 to turn exclusively on or every one of the PMOS transistors QP1 – QPn-1 to turn off and one of the NMOS transistors QN1 – QNn to turn exclusively off, in accordance with the externally input voltage switching signal Sc.

[0058] As described above, in each power supply apparatus 1, 1a, 1b, and 1c, the voltage dividing circuit 5 is configured to have a feedback circuit for dividing the output voltage Vo to generate the divided voltage Vd. This voltage dividing circuit 5 is

further configured to change the voltage dividing ratio relative to the output voltage Vo in accordance with the voltage switching signal Sc to change consequently the divided voltage Vd. Thereby, the voltage value of the output voltage Vo is changed in a preferable manner. In other words, each power supply apparatus 1, 1a, 1b, and 1c has the structure capable of allowing an external selection of the output voltage Vo from a plurality of predetermined voltage values. Therefore, any one power supply apparatus 1, 1a, 1b, and 1c can comply with a change in the power requirements of the load circuit by easily changing the output voltage value without the needs of changing the power supply apparatus itself.

[0059] In addition, in any one power supply apparatus 1, 1a 1b, and 1c, each of the resistors RB1 – RBn coupled to the NMOS transistors QN1 – QNn, respectively, is turned into conductive status when corresponding one of the NMOS transistors QN1 – QNn is turned off into non-conductive status. That is, a parasitic capacitor of each resistor can be disregarded in the status that the NMOS transistor is out of conduction. This status facilitates a phase design of the voltage dividing circuit 5.

[0060] Referring to FIG. 8, a power supply apparatus 51 according to another preferred embodiment of the present invention is explained. FIG. 8 shows the power supply apparatus 51 which is similar to the power supply apparatus 1 of FIG. 2, having a DC-to-DC (direct current to direct current) converter including a voltage-step-down-type switching regulator, except for a voltage dividing circuit 52. As shown in FIG. 8, the power supply apparatus 51 is connected to the direct current power source 10, and includes the switching transistor 2, the smoothing circuit 3, the reference voltage generator 4, the voltage dividing circuit 52, the error amplifier 6, and the control circuit 7.

[0061] The voltage dividing circuit 52 includes a voltage divider 61 and a switching controller 62. The voltage divider 61 switches a dividing ratio in accordance with an input control signal, and accordingly generates and outputs the divided voltage Vd. The switching controller 62 controls the switching of the dividing ratio of the voltage

divider 61 in accordance with a voltage switching signal Sc which is externally input thereto.

[0062] FIG. 9 breaks down the voltage divider 61 of the voltage dividing circuit 52 and, with reference thereto, an exemplary operation of the voltage dividing circuit 52 is explained. The voltage divider 61 includes n resistors referred to as resistors RC1 – RCn, n resistors in series referred to as resistors RD1 – RDn, n PMOS transistors referred to as PMOS transistors QP1 – QPn, (n–1) N-channel MOS transistors referred to as NMOS transistors QN1 – QNn-1, and a capacitor 16. The resistors RC1 – RCn are configured as a first resistor circuit, the resistors RD1 – RDn are configured as a second resistor circuit, the PMOS transistors QP1 – QPn are configured as a first switching circuit, and the NMOS transistors QN1 – QNn-1 are configured as a second switching circuit.

[0063] The resistors RD1 – RDn are connected in series between an output terminal 65 of the voltage dividing circuit 61 and the ground. The NMOS transistors QN1 – QNn-1 are coupled to the resistors RD1 – RDn-1, respectively, to form n-1 sets of transistor-resistors parallel circuits, which are connected in series between the output terminal 65 and the ground. The switching controller 62 generates control signals SN1 – SNn based on the voltage switching signal Sc, and applies the control signals SN1 – SNn-1 to gates of the NMOS transistors QN1 – QNn-1, respectively.

[0064] The capacitor 16 is also connected between the output terminal OUT of the power supply apparatus 51 and the output terminal 65. The PMOS transistors QP1 – QPn are coupled to the resistors RC1 – RCn, respectively, to form n sets of transistor-resistor series circuits, which are connected in parallel between the output terminal OUT of the power supply apparatus 51 and the ground. The control signals SN1 – SNn of the switching controller 62 are also applied to gates of the PMOS transistors QP1 – QPn, respectively.

[0065] The switching controller 62 drops one of the control signals SN1 – SNn down to the level L and raises the rest of the control signals to the level H in accordance with the externally input voltage switching signal Sc. For example, when the

control signal SNm is dropped down to the level L and the rest of the control signals are raised to the level H, the PMOS transistor QPm is selected among the PMOS transistors QP1 – QPn to be turned on to be conductive and the rest of the PMOS transistors are turned on to be non-conductive, where m is an integer between 1 and n-1. At the same time, the NMOS transistor QNm is selected among the NMOS transistors QN1 – QNn-1 to be turned off to be non-conductive and the rest of the NMOS transistors are turned on to be conductive. Thereby, the resistor RCm is connected between the output terminal OUT and the output terminal 65, and the resistors RDm and RDn are connected in series between the output terminal 65 and the ground.

[0066] When the above-described conditions are established, the divided voltage Vd is expressed by a third equation; $Vd=Vo \times (RDm+RDn)/(RCm+RDm+RDn)$, where RCm, RDm, and RDn represent values of the resistors RCm, RDm, and RDn, respectively.

[0067] The input voltages to the inverse and non-inverse input terminals of the error amplifier 6, which are Vd and Vr, respectively, are equalized due to the imaginary short phenomenon occurring therebetween. That is, in this case, a relationship between Vd and Vr is expressed as $Vd=Vr$. Therefore, the above third equation can be modified as; $Vo=Vr \times (RCm+RDm+RDn)/(RDm+RDn)$.

[0068] As another example, when the control signal SNn is dropped down to the level L and the control signals SN1 – SNn-1 are raised to the level H, the PMOS transistors QP1 – QPn-1 are turned off to be non-conductive. At the same time, the PMOS transistor QPn is turned on to be conductive and the NMOS transistors QN1 – QNn-1 are turned on to be conductive. Thereby, the resistor RCn is connected between the output terminal OUT and the output terminal 65, and the resistor RDn is connected between the output terminal 65 and the ground.

[0069] Under the above-mentioned conditions, the divided voltage Vd is expressed by a fourth equation; $Vd=(Vo \times RDn)/(RCn+RDn)$, where RCn represents a value of the resistor RCn.

[0070] The input voltages to the inverse and non-inverse input terminals of the error amplifier 6, which are Vd and Vr, respectively, are equalized due to the imaginary short phenomenon occurring therebetween. That is, in this case, a relationship between Vd and Vr is expressed as Vd=Vr. Therefore, the above fourth equation can be modified as; Vo=Vr x (RCn+RDn)/RDn.

[0071] In this way, the voltage divider 51 can vary the value of the output voltage Vo in accordance with the voltage switching signal Sc. In other words, a desirable value of the output voltage Vo can be obtained from the voltage divider 51 by suitably selecting the voltage switching signal Sc.

[0072] FIG. 10 shows an exemplary circuit of the voltage dividing circuit 52 when n is two. In the voltage dividing circuit 52 of FIG. 10, the PMOS transistors QP1 and QP2 are coupled to the resistors RC1 and RC2, respectively, to form two pieces of transistor-resistor series circuits which are connected in parallel between the output terminal OUT and the output terminal 65. Also, the capacitor 16 is connected between the output terminal OUT and the output terminal 65.

[0073] Further, the resistors RD1 and RD2 are connected between the output terminal 65 and the ground, and the NMOS transistor QN1 is coupled to the resistor RD1 to form a transistor-resistor series circuit which is connected in series to the resistor RD2 between the output terminal 65 and the ground. The switching controller 62 includes an inverter 67, and generates the control signals SN1 and SN2 based on the voltage switching signal Sc. The control signal SN1 is a straight signal of the voltage switching signal Sc as it is and the control signal SN2 is an inverted signal of the voltage switching signal Sc. The control signal SN1 is applied to the gates of the PMOS transistor QP1 and the NMOS transistor QN1, and the control signal SN2 is applied to the gate of the PMOS transistor QP2.

[0074] In the voltage dividing circuit 52 of FIG. 10, the output voltage Vo based on the above modified third equation can be expressed as;
Vo=Vr x (RC1+RD1+RD2)/(RD1+RD2).

[0075] Also, the above modified fourth equation can be expressed as; Vo=Vr x (RC2+RD2)/RD2.

[0076] In the power supply apparatus 1 of FIG. 8, the reference voltage generator 4, the voltage dividing circuit 52, the error amplifier 6, and the control circuit 7 are integrated into one IC (integrated circuit) chip. It is possible to further integrate the switching transistor 2 into that IC chip.

[0077] It is also possible to substitute an NMOS transistor for the flywheel diode D1. FIG. 5 shows a power supply apparatus 1a which is a first modified version based on the power supply apparatus 1 of FIG. 2, in which the flywheel diode D1 is substituted by an NMOS transistor, as in the case of FIG. 5. In this case, it becomes possible to integrate the switching transistor 2, the reference voltage generator 4, the voltage dividing circuit 52, the error amplifier 6, the control circuit 7, and the NMOS transistor into one IC (integrated circuit) chip.

[0078] To use a DC-to-DC (direct current to direct current) converter including a voltage-step-up-type switching regulator as an alternative to the DC-to-DC converter including the voltage-step-down-type switching regulator, the power supply apparatus 51 of FIG. 8 may become the one similar to the power supply apparatus 1b shown in FIG. 6, except that the voltage dividing circuit 5 is replaced with the voltage dividing circuit 52. In such a power supply apparatus, the reference voltage generator 4, the voltage dividing circuit 52, the error amplifier 6, and the control circuit 33 can be integrated into one IC (integrated circuit) chip. It is also possible to further integrate the switching transistor 31 into that IC chip.

[0079] Further, to use a series regulator instead of a switching regulator, the power supply apparatus 51 of FIG. 8 may become the one similar to the power supply apparatus 1c shown in FIG. 7, except that the voltage dividing circuit 5 is replaced with the voltage dividing circuit 52. In such a power supply apparatus, the reference voltage generator 4, the voltage dividing circuit 52, and the error amplifier 6 can be integrated into

one IC (integrated circuit) chip. It is also possible to further integrate the output control transistor 41 into that IC chip.

[0080] In the power supply apparatus 51 of FIG. 8, the switching controller 62 of the voltage dividing circuit 52 causes one of the PMOS transistors QP1 – QPn to turn exclusively on and one of the NMOS transistors QN1 – QNn-1 to turn exclusively off or every one of the NMOS transistors QN1 – QNn-1 to turn on, in accordance with the externally input voltage switching signal Sc, as one example.

[0081] As an alternative, the switching controller 62 may cause more than one of the PMOS transistors QP1 – QPn to turn on simultaneously and more than one of the NMOS transistors QN1 – QNn-1 to turn off simultaneously, in accordance with the externally input voltage switching signal Sc.

[0082] As another alternative, the switching controller 12 may cause one of the PMOS transistors QP1 – QPn to turn exclusively off and one of the NMOS transistors QN1 – QNn-1 to turn exclusively on or every one of the NMOS transistors QN1 – QNn-1 to turn off, in accordance with the externally input voltage switching signal Sc.

[0083] As described above, in the power supply apparatus 51, the voltage dividing circuit 52 is configured to have a feedback circuit for dividing the output voltage Vo to generate the divided voltage Vd. This voltage dividing circuit 52 is further configured to change the voltage dividing ratio relative to the output voltage Vo in accordance with the voltage switching signal Sc to change consequently the divided voltage Vd. Thereby, the voltage value of the output voltage Vo is changed in a preferable manner. In other words, each one of the power supply apparatus 51 has the structure capable of allowing an external selection of the output voltage Vo from a plurality of predetermined voltage values. Therefore, the power supply apparatus 51 can comply with a change in the power requirements of the load circuit by easily changing the output voltage value without the needs of changing the power supply apparatus itself.

[0084] While the invention has been described and illustrated with reference to specific exemplary embodiments, it should be understood that many modifications and substitutions can be made without departing from the spirit and scope of the invention. Accordingly, the invention is not to be considered as limited by the foregoing description but is only limited by the scope of the appended claims.